CS-01-193

January 13, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/697,746 10/30/03

Tze Ho Chan et al.

METHOD TO SELECTIVELY FORM POLY SiGe P TYPE ELECTRODE AND POLY-SILICON N TYPE ELECTRODE THROUGH PLANARIZATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

The following three U.S. Patents disclose dual gate oxide processes:

1) U.S. Patent 6,358,819 to Shelton et al., "Dual Gate Oxide Process for Deep Submicron ICs."

2) U.S. Patent 5,918,116 to Chittipeddi, "Process for Forming Gate Oxides Possessing Different Thicknesses on a Semiconductor Substrate."

3) U.S. Patent 6,063,670 to Lin et al., "Gate Fabrication Processes for Split-Gate Transistors."

U.S. Patent 6,342,438 to Yu et al., "Method of Manufacturing a Dual Doped CMOS Gate," teaches doping PMOS and NMOS regions differently before patterning polysilicon gates.

U.S. Patent 5,356,821 to Naruse et al., "Method for Manufacturing Semiconductor Integrated Circuit Device," discloses epitaxial growth of SiGe gates for both NMOS and PMOS.

U.S. Patent 6,376,323 to Kim et al., "Fabrication of Gate of P-Channel Field Effect Transistor with Added Implantation Before Pattering of the Gate," teaches PolySiGe gates for both PMOS and NMOS with selective doping.

CS-01-193

CS-01-093 serial number 10/266,425, filed 10/08/02, to Chew-Hoe Ang et al., "Dual Si-Ge Polysilicon Gate with Different Ge Concentrations for CMOS Device Optimization," discloses a method for forming SiGe gates having different Ge concentrations for PMOS and NMOS.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS-01-193	10/697,746
Applicant: Tze Ho Chan et al.	
Filing Date: 10/30/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6358819	3/19/02	Shelton et al.	438	433	12/15/98
	5918116	6/29/99	Chittipeddi	438	199	5/9/97
	6063705	5/16/00	Lin et al.	438	275	4/15/98
	6342438	1/29/02	Yu et al.	438	520	11/6/98
	5356821	10/18/94	Naruse et al.	437	34	8/12/93
	6376323	4/23/02	Kim et al.	438	373	4/4/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

-	CS-01-093 Serial No. 10/266,425, Filed 10/08/02 to Chew-Hoe Ang et al., "Dual Si-Ge Polysilicon Gate with Different Ge Concentrations for CMOS Device Optimization".

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.